ELLIOTT 900

Volume 4: ENGINEERING MAINTENANCE

Part 1: BASIC EQUIPMENT

Section 4: TELEPRINTER (DPA 211 and 241)

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Chapter 1: INTRODUCTION

1.1 Location of Component Parts.

The teleprinter is a type 33 which is mounted on its own stand and usually positioned by the side of the central processor desk. The teleprinter incorporates a reader and punch, which will be called the printer reader and printer punch, to avoid confusion with the tape reader and tape punch which may be used in conjunction with the teleprinter.

The power supply unit, with its associated control circuitry, and the rack containing the logic boards are mounted in the left hand side of the processor desk. The operators controls are located on the teleprinter and on a panel housed along the top front edge of the desk.

Views of the teleprinter controller in the processor desk are shown in Figure 1.

1.2 Connections.

The cables linking the units within the teleprinter controller, the mains input from the filter unit and the connection to the interface are shown in Figure 2.

1.3 Logic Boards.

The circuits of the L. S. A. elements used on the logic boards are described in Section 1 of this Part of the Manual. The tables in Figure 8 provide details of the types of L. S. A. element on each board and the location and value of any extra components used.

Descriptions of the special circuits located on board DPS 14, in position 25 of the logic rack, are contained in Chapter 5.

On the logic diagrams Figures 5, 6 and 7, signals to and from the central processor are enclosed in square brackets [ ] and signals to and from the teleprinter are enclosed in diamond brackets < > . All discrete components, not being part of the sub-assemblies, are fitted in Area G of the logic board.

Chapter 2: POWER DISTRIBUTION

2. 1 Introduction.

The power distribution is shown in Figures 3 and 4. The control station is wired so that it can accommodate the teleprinter plus a tape punch and tape reader. When a full system is not used, the logic boards associated with the missing devices are omitted. The Figures in this section show the complete wiring and are not isolated to that used by the teleprinter.

2. 2 A. C. Supplies.

The distribution of the a. c. supplies is shown in Figure 3.

The mains input on TB1 is taken to the contacts of RLA. This relay is energised by a 24V signal from the interface which is present when the mains ON button on the control unit is operated. A Local/Remote switch is available to by-pass the relay contacts when required.

2. 3 D. C. Supplies.

The distribution of the d. c. supplies is shown in Figure 4.

The d. c. supplies are produced by two units labelled PSA and PSB. PSA is a type NS-ELL/006 catalogue No. 11224 and provides the +6V and -6V supplies at current ratings of 3A and 1A respectively. PSB is a type ES 1000/28, catalogue No. 11225, and provides the +28V supply at a current rating of 10A.

Details of these units can be obtained from the manufacturers handbooks.

2.4 Over-Voltage Protection

An over-voltage protection circuit is connected across the +6V and -6V d.c. outputs to protect the logic boards from damage due to a rise in level of either of these supplies. Under normal operating conditions, the lamps will be lit and no current taken by the circuit.

If either of the d.c. outputs start to rise then current will be drawn through the corresponding zener diode and current applied to the thyristor. Dependent on the ambient temperature and component tolerances, the thyristor will be triggered when the d.c. level has risen to a value between 6.5V and 10.0V.

When the thyristor conducts, the output terminals of the power unit are short circuited causing the appropriate fuse to blow and the lamp to extinguish.

2.5 Hour Meter

To measure the total time that the computer is switched on, an Hour Meter can be provided as an optional facility. This is located on the rear of the power supply unit as shown in Figure 1.

The meter is connected to TB1 pins 4 and 5, the same pins as feed the a.c. mains supply to the paper tape reader. When the ON button on the Control Unit is pressed, the processor power supplies are up-sequenced and a 24V signal is sent to the paper tape station to energise RLA (Figure 3). The contacts of RLA connect the a.c. mains to the Teleprinter and Reader (if fitted) and hence cause the Hour Meter to be energised.

Chapter 3: TELEPRINTER INPUT

3.1 Introduction.

This chapter contains a functional description of the control logic associated with the teleprinter when used to input a character into the central processor. The logic is shown in Figures 5 and 6. The character can originate from the keyboard or the printer reader, in either case a common input line carries the information to the logic.

It is assumed throughout that the reader is familiar with the appropriate specifications in Volume 1 of the Manual.

3.2 Basic Cycle.

Assuming that the teleprinter is not busy, a brief description of the normal transfer cycle is as follows.

On receipt of an input selection signal the Demand lamp lights. When a key is pressed or the printer reader started, a serial character is produced and fed to the logic. The first pulse of the character is used as a starting signal for a clock which produces pulses to cause the character to be loaded in a serial fashion into a buffer register. The character is also fed back to the teleprinter to operate the typing mechanism and, if required, the printer punch.

When the character is in the correct position in the buffer, the clock is stopped and further characters from the teleprinter inhibited. The input selection signal is now accepted by the interface logic and a timing sequence initiated to gate the data from the register onto the interface lines.

After the data has been accepted by the central processor, the input selection signal is removed, the Demand lamp goes off, and the logic is reset ready to accept the next data transfer.

3.3 Channel Selection.

An input from the teleprinter is selected according to the position of the Select In switch and/or the type of system in use. For an input to be taken from the teleprinter, TIN must be true.

If a tape reader and tape punch are not used, the associated logic is omitted and the READ and PUNCH LINKS on boards 5 and 11 respectively will not be present. This means that the inputs to 14/1B11 and 14/1B12 are at a true level and will always hold TIN true and RIN false. Under these circumstances the position of the Select In switch has no effect on the logic and all inputs must come from the teleprinter.

When a tape reader and tape punch are used with the system, the READ and PUNCH LINKS are present. In this case TIN will be true and RIN false when the Select In switch is set to TELEPRINTER, or to AUTO with the interface signal [ADDRESS BIT 3] true. At all other times TIN will be false and RIN true.

3.4 Character from Teleprinter.

A character from the teleprinter, whether derived from the keyboard or the printer reader, is approximately 100 ms long when the teleprinter is operating at 10 characters/second, and consists of eleven pulses.

The character is sent to the logic in serial form, and when viewed at the output of the line receiver 23/6B12, the first pulse is always true and is called the Start pulse. The next eight pulses contain the code of the character and may be either true or false according to the code combination. The last two pulses are always false and are called the Stop pulses. The output then remains false until the next character is sent.

3. 5 Teleprinter Clock.

3. 5. 1 Clock Pulses.

The clock pulses $\overline{S1}$ and $\overline{S2}$ are used to strobe the data along the register during both input and output modes of operation. The timing is arranged so that $\overline{S1}$ and $\overline{S2}$ are produced alternately with a period of 4. 55 ms between each pulse. The timing of the clock is shown in Figure 7.

The logic for the clock is located on DPS14 and DP18 in positions 25 and 23 respectively of the logic rack and is shown in Figure 7.

3. 5. 2 Initial Conditions.

When a data transfer is not in progress the clock is not running and all inputs to 25/2B12 are at a true level. This causes the output to be false and hence CLOCK BUSY, the output of 23/6A13 is also false.

The bistable 23/3A/2A is set by the false output of the pulse generator 23/3B11 and CLOCK BUSY such that the output of 23/3A12 is true.

3. 5. 3 Operation of Clock.

The conditions required for the clock to start are that all inputs to 25/2A12 must be true, causing the output to go false. This triggers the pulse generator 25/3A11 to produce a 330 ns pulse to open gate 25/4A12 and cause $\overline{TIME1}$ to go false. $\overline{TIME1}$ is inverted by 25/4A13 and used to fire the special pulse generator which produces an accurate 2. 27 ms pulse. This pulse applied to 25/4A12 holds $\overline{TIME1}$ at a false level for 2. 27 ms.

$\overline{TIME1}$ fed to 25/2B12 causes CLOCK BUSY to go true.

$\overline{\text{TIME1}}$ is also inverted by 25/2A11 and applied to the pulse generator 25/3A13. At the end of $\overline{\text{TIME1}}$ this pulse generator is triggered and a 330 ns pulse produced. This is the COUNT pulse and is used for two purposes.

The COUNT pulse is applied to 25/4B12 to cause $\overline{\text{TIME2}}$ to go false. $\overline{\text{TIME2}}$ is held fase by 25/4B13 and the special 2.27 ms pulse generator.

The COUNT pulse is inverted by 23/2B11 and applied to the two pulse generators 23/3B11 and 23/3B13. The outputs of the bistable 23/3A/2A are also fed to the pulse generators and as the output 23/2A12 is false then 23/3B13 is not triggered. The pulse from 23/3B11 sets the bistable causing the output of 23/3A12 to go false.

$\overline{\text{TIME2}}$ is fed to 25/2B11 and is also used to ensure that CLOCK BUSY remains true. At the end of the 2.27 ms $\overline{\text{TIME2}}$ pulse the output of 25/2B11 goes false to trigger the pulse generator 25/3B13 to produce the 10μs SHIFT pulse. This pulse is gated with the outputs of the bistable 23/3A/2A and $\overline{\text{S1}}$ is produced from 23/2A13.

Shift is also inverted by 25/2A13 and fed to the gate 25/2A12 causing its output to go true. At the end of the SHIFT pulse the output of 25/2A12 goes false to initiate a further cycle of the clock.

During the next cycle the COUNT pulse will trigger pulse generator 23/3B13 to reset the bistable 23/3A/2A such that the output of 23/3A12 is true. The SHIFT pulse will therefore produce $\overline{\text{S2}}$ from 23/3A13.

The clock continues to produce $\overline{\text{S1}}$ and $\overline{\text{S2}}$ pulses until the character shift is complete and RUN goes false. This holds the output of 25/2A12 at a true level and prevents further triggering of the clock.

When the last $\overline{\text{SHIFT}}$ pulse goes true, CLOCK BUSY goes false to reset the bistable 23/3A/2A such that the output of 23/3A12 is true. This ensures that when the clock is restarted, $\overline{\text{S1}}$ will be the first pulse produced.

3.6 Teleprinter Input Timing.

3.6.1 Demand Signal.

When an input is required by the central processor, interface signal [STR] goes true and hence $\overline{\text{INSEL}}$ goes false. RIN is false when the teleprinter is selected, and this signal with $\overline{\text{INSEL}}$ causes the Demand lamp to light via the logic element 15/4B. The Demand lamp is located on the control panel.

3.6.2 INFO

When a key is pressed or the printer reader is started, a character will be produced by the teleprinter (see para. 3.4) and sent in serial fashion to the line receiver 23/6B12.

The two signals $\overline{\text{RESET}}$ and $\overline{\text{BLOCK}}$ are true and the outputs of 23/4B13 and 23/5B11 are both false, holding 23/5A12 true. The Start pulse causes $\overline{\text{INFO}}$, the output of 23/6A12, to go false. This signal is inverted by 23/5A13 to produce INFO.

In the input mode of operation, the INFO signal is identical to the character generated by the teleprinter mechanism. The signal is re-input to the teleprinter via the line transmitter 23/7B13 to operate the typing mechanism and, if required, the printer punch.

3. 6. 3 Starting the Clock.

INFO is gated at 22/2A11 with $\overline{\text{BLOCK}}$ and $\overline{\text{TDOUT}}$, both of which are true, causing the output to go false. This in turn sets the bistable 22/2A/2B causing R to go true and $\overline{R}$ false.

$\overline{R}$ going false causes RUN, the output of 22/3B13, to go true. RUN is fed to 25/2A12 which is the gate controlling the running of the clock. The other three inputs are true so that RUN going true causes the output of 25/2A12 to go false and start the clock running. The operation of the clock is described in para. 3. 5.

$\overline{R}$ is also fed to 22/5A11 causing CLEAR to go false so that data can be loaded into the buffer register.

3. 6. 4 Loading the Register.

The register consists of eleven stages, each comprising two bistables, located on boards 19, 20 and 21 of the logic rack. The first of the bistables in each stage is strobed by the $\overline{S1}$ pulse and the second bistable in each stage by the $\overline{S2}$ pulse. The serial characters INFO and $\overline{\text{INFO}}$ are fed to 19/1A12 and 19/1A13 respectively and by the strobing action of the clock pulses are moved along the register from left to right.

When the register is not being used, it is held in the reset state by the CLEAR signal being true. This means that the top output of each stage, $\overline{ST}$ on the eleventh stage, is at a true level, and the lower output, ST on the eleventh stage, at a false level.

The character is moved to the right by the strobing action of the clock pulses until the tenth $\overline{S1}$ pulse occurs. At this point the Start pulse of the character will be gated by $\overline{S1}$ at 21/4B12 causing the output to go false. This signal is inverted by 21/4A13 causing STOP I/P to go true.

3.6.5 Stopping the Clock.

STOP I/P is gated with $\overline{L}$* and R at 22/1B11 causing the output to go false. This sets the bistable 22/1A/1B causing $\overline{L}$ to go false. $\overline{L}$* also goes false to reset the bistable 22/2B/2A causing $\overline{R}$ to go true and R false. With $\overline{R}$ going true, RUN goes false and inhibits further start pulses for the clock at 25/2A12.

$\overline{L}$ applied to 22/4B12 and $\overline{R}$ applied to 22/5B11 cause BLOCK, the output of 22/5B12 to go true. $\overline{BLOCK}$ the output of 22/5B13 applied to 23/6A12 holds its output at a true level. If a key is pressed the character is inhibited at 23/6A12 by $\overline{BLOCK}$ and also gated with BLOCK at 23/4A12 causing the output to go false. This false output triggers the pulse generator 23/4B13 and causes the output of the regenerable monostable 23/5B11 to go true. These signals cause the output of 23/5A12 to go false and enforce the inhibit on 23/6A12. The regenerable monostable has a recovery time of 200 ms, so that this period must elapse after BLOCK has gone false before a character is allowed to pass to the INFO state.

$\overline{BLOCK}$ also inhibits any spurious INFO signals at 23/7B13 and 22/2A11.

$\overline{L}$ going false and applied to 22/5A12 ensures that CLEAR remains false and the register is not reset.

When R goes false, the pulse generator 23/1A13 is triggered, the resultant 10 ms pulse is used to inhibit spurious pulses to the teleprinter from the $\overline{ST}$ line at 23/1B12. The pulse is inverted by 23/1B13 to produce $\overline{INH}$. This pulse is applied to 25/2A12 to prevent the clock from starting, and to 22/3B12 to hold TWAIT true.

3.6.6 Data Transfer.

As RUN, CLOCK BUSY and $\overline{L}$* are false, when $\overline{INH}$ goes true at the end of the 10 ms pulse, TWAIT goes false.

With the teleprinter selected RIN is false and TIN true, so that TWAIT going false causes $\overline{INBUSY}$, the output of 16/2A12, to go true. As INSEL is true the output of 16/1A12 goes false to set the bistable 16/4A/4A causing $\overline{ACT}$ to go false. A 1μs delay is introduced before $\overline{ACT1}$ goes false and triggers the monostable 16/5B/4B to produce 680 ns pulses ACT* and $\overline{ACT}$*. The 1μs delay is produced by the capacitor to earth and is to prevent small spikes propagating spurious ACT* and ACT** pulses. The 680 ns pulse ACT** generated by 16/7B13 sets the bistable 16/2B/2B to send a true [RTR] signal down the interface line.

$\overline{ACT1}$ is inverted by 16/7A12 to produce YES which is in turn gated with TIN and INSEL to give a false $\overline{TDIN}$ signal from 15/2B11 and a true TDIN signal from 15/1B11.

ACT* and TDIN applied to 22/1A12 causes $\overline{RESETL}$ to go false for 680 ns to reset the bistable 22/1B/1A causing $\overline{L}$ and $\overline{L}$* to go true. BLOCK is held true and CLEAR false by $\overline{TDIN}$ applied to 22/4B12 and 22/5A12 respectively. $\overline{L}$* applied to 22/3B11 causes TWAIT to go true.

When the input to the register was stopped the data is present on the outputs of the left hand eight stages of the register. The data is applied to the gates 1A etc. on board 15 and when TDIN goes true this data is strobed onto the interface lines [IR1] to [IR8] via the line transmitters 14/1A11 etc.

After the data has been accepted by the central processor, [STR] goes false causing SELECT, the output of 16/1A13, to go false and reset the bistables 16/4A/4A and 16/2B/2B. $\overline{\text{ACT1}}$ goes true causing $\overline{\text{TDIN}}$ to go true.

With $\overline{\text{TDIN}}$ going true, CLEAR goes true to reset the buffer register, and BLOCK goes false to enable a further character to be input.

3.7 Reset Signals.

3.7.1 $\overline{\text{RESET}}$

This signal from 15/7A13 is derived from the [RESET] signal generated in the central processor. The $\overline{\text{RESET}}$ signal goes false when the equipment is first switched on and also when the Reset button is operated. The signal remains false until the Jump button is pressed.

The $\overline{\text{RESET}}$ signal has four uses.

(1) Applied to bistable 22/1B/1A it ensures that $\overline{\text{L}}$ is true.

(2) Applied to bistable 22/3A/3A it ensures that $\overline{\text{O}}$ is true.

(3) Applied to 22/2B11 it ensures that the bistable 22/2B/2A is set such that $\overline{\text{R}}$ is true.

(4) Applied to 23/6A12 it ensures that INFO is held false.

3.7.2 RESET

This is the inverse of $\overline{\text{RESET}}$ and is obtained from 15/7A11. It is applied to 22/5A11 to hold CLEAR true and the register in a reset state.

Chapter 4: TELEPRINTER OUTPUT

4. 1 Introduction.

This chapter contains a functional description of the control logic associated with the teleprinter when used as an output device for a character from the central processor. The logic is shown in Figures 5 and 6. The character is typed by the keyboard printer and, if required, can be reproduced on tape by the printer punch.

It is assumed throughout that the reader is familiar with the appropriate specifications in Volume 1 of this Manual.

4. 2 Basic Cycle.

Assuming that the teleprinter is not busy, a brief description of the normal transfer cycle is as follows.

The teleprinter logic accepts the output selection signal from the central processor and starts a timing chain which gates the data into the buffer register and sends a reply to the processor.

When the output selection signal is removed, the clock is started and a series of strobing pulses produced. These pulses shift the character to the right and it is fed serially to the teleprinter mechanism. When the character has been completely transferred, the clock is stopped and the logic reset ready to accept the next data transfer.

4. 3 Channel Selection.

An output to the teleprinter is selected according to the position of the Select Out switch and/or the type of system in use. For an output to be sent to the teleprinter, TOUT must be true.

If a tape reader and tape punch are not used, the associated logic is omitted and the READ and PUNCH links on boards 5 and 11 respectively will not be present. This means that the inputs to 14/1B13 and 14/3B11 are always at a true level and will hold TOUT true and POUT false. Under these circumstances the position of the Select Out switch has no effect on the logic and all outputs go to the teleprinter. ;

When a tape reader and tape punch are used with the system, the READ and PUNCH links will be present. In this case TOUT will be true and POUT false when the Select Out switch is set to TELEPRINTER, or to AUTO with the interface signal [ADDRESS BIT 3] true. At all other times TOUT will be false and POUT true.

4.4 Teleprinter Output Timing.

4.4.1 Data to Register.

When data is to be output from the central processor, the interface signal [STP] goes true. This causes $\overline{\text{OUTSEL}}$ to go false and hence TWAIT, the output of 22/3B12, also goes false. With the teleprinter selected, TOUT is true and POUT false, thus TWAIT going false causes $\overline{\text{OUTBUSY}}$ to go true and accept the OUTSEL signal.

The output of 16/1A12 going false sets the bistable 16/4A/4A causing $\overline{\text{ACT}}$ to go false. A 1μs delay is introduced before $\overline{\text{ACT1}}$ goes false and triggers the monostable 16/5B/4B to produce 680 ns pulses ACT* and $\overline{\text{ACT}}$*. The 1μs delay is produced by the capacitor to earth and is to prevent small spikes propagating spurious ACT* and ACT** pulses. The 680 ns pulse ACT** generated by 16/7B13 sets the bistable 16/2B/2B to send a true [RTR] signal down the interface line.

OUTSEL and TOUT going true cause $\overline{\text{TDOUT}}$, the output of 15/3B13, to go false. This signal is inverted by 22/4A11 to produce TDOUT. $\overline{\text{ACT}}$ is inverted by 22/4A13 and gated with TDOUT to cause $\overline{\text{RESETL}}$, the output of 22/1A12, to go false. $\overline{\text{RESETL}}$ is applied to 25/2A12 to prevent the clock from starting until data is transferred to the buffer. The signal applied to 22/4B12 causes $\overline{\text{BLOCK}}$ to go false and this signal inhibits INFO at 23/6A12 and 23/7B11. $\overline{\text{RESETL}}$ inhibits $\overline{\text{ST}}$ signals at 23/7B11.

ACT* is gated with TDOUT at 22/4A12 to produce the 680 ns pulse $\overline{\text{TDOUT}}$*. This pulse sets the bistable 23/3A/3A causing O to go true and $\overline{\text{O}}$ false. $\overline{\text{TDOUT}}$* is inverted by 19/5A12, 20/7B11 and 21/7B11 and gated with the data signals $\overline{\text{OUT1}}$ to $\overline{\text{OUT8}}$ to transfer the information to the register.

The O signal applied to 23/4A13 causes $\overline{\text{INFO}}$ to be held false and INFO true.

The $\overline{\text{O}}$ signal applied to 22/5A12 causes CLEAR to go false and allow data to be entered into the register. $\overline{\text{O}}$ applied to 22/4B12 ensures that $\overline{\text{BLOCK}}$ remains false and applied to 25/2B12 causes CLOCK BUSY to go true. $\overline{\text{O}}$ is also applied to 22/3B13 causing RUN to go true and hence TWAIT to go true.

4.4.2 Strobing Register.

After the [RTR] signal is received by the central processor, the [STP] signal goes false. This resets the bistables 16/4A/4A and 16/2B/2B in the timing chain and causes $\overline{\text{TDOUT}}$ to go true. This in turn causes $\overline{\text{RESETL}}$ to go true and the clock is allowed to start. The operation of the clock is described in para. 3.5.

The Inputs to 23/7B11 are $\overline{\text{BLOCK}}$ which is false, INFO, O and $\overline{\text{RESETL}}$ which are true and the output to the teleprinter mechanism is thus controlled by $\overline{\text{ST}}$.

With the clock running, the $\overline{\text{S1}}$ and $\overline{\text{S2}}$ pulses move the data from left to right along the register. The extreme right hand stage has no data input (21/6A13) and this causes $\overline{\text{ST}}$ to be false for the first 9.1 ms period. This is used as a Start pulse for the teleprinter mechanism, so that the format of the character is identical to that produced in the input mode of operation. The level of $\overline{\text{ST}}$ will subsequently depend on the code of the character output from the processor.

Since INFO is held true and $\overline{\text{INFO}}$ false, then each $\overline{\text{S1}}$ pulse gates a true and false level respectively into the left hand end of the register. When the character has been completely shifted, the lower output of each stage of the register is at a true level. These outputs are gated in pairs at 21/7B12, 21/7A12, 20/7B12 and 20/7A12 to produce signals $\overline{\text{END D}}$, $\overline{\text{END C}}$, $\overline{\text{END B}}$ and $\overline{\text{END A}}$ respectively. These four signals with the three stage outputs of board 19, $\overline{\text{A}}$, $\overline{\text{B}}$ and $\overline{\text{C}}$, are gated together at 19/6A and 19/6B. When all stage outputs are true, END O/P goes true.

END O/P resets the bistable 22/3A/3A causing O to go false and $\overline{\text{O}}$ true.

With $\overline{\text{O}}$ going true, RUN goes false to prevent further clock pulses. CLEAR goes true to reset the register and $\overline{\text{BLOCK}}$ goes true. CLOCK BUSY goes false at the end of the SHIFT pulse to reset the bistable 23/2A/3A as described in paragraph 3.5.

With O going false, $\overline{\text{ST}}$ signals are blocked at 23/7B11, and INFO goes false.

The logic is now in a ready state to accept the next data transfer.

4.5 Reset Signals.

4.5.1 $\overline{\text{RESET}}$

This signal from 15/7A13 is derived from the [RESET] signal generated in the central processor. The $\overline{\text{RESET}}$ signal goes false when the equipment is first switched on and also when the Reset button is operated. The signal remains false until the Jump button is pressed.

The $\overline{\text{RESET}}$ signal has four uses:

(1) Applied to bistable 22/1B/1A it ensures that $\overline{\text{L}}$ is true.

(2) Applied to bistable 22/3A/3A it ensures that $\overline{\text{O}}$ is true.

(3) Applied to 22/2B11 it ensures that the bistable 22/2B/2A is set such that $\overline{\text{R}}$ is true.

(4) Applied to 23/6A12 it ensures that INFO is held false.

4.5.2 RESET

This is the inverse of $\overline{\text{RESET}}$ and is obtained from 15/7A11. It is applied to 22/5A11 to hold CLEAR true and the register in a reset state.

Chapter 5: SPECIAL CLOCK CIRCUITS

5.1 Introduction

The teleprinter clock board DPS14 in position 25 of the logic rack contains two special circuits. Areas D and C each contain a high stability 2.27 ms pulse generator. In area E is located a stabiliser which provides a + 10V d.c. supply for the pulse generators. The remainder of the board contains L.S.A. elements.

The component layout on the board is shown in Figure 9, together with the circuit diagrams and component tables for the two special circuits.

5.2 Pulse Generator.

When not in operation the input is held at a false level and VT1 is reverse biased. C1 is not charged and VT2 conducts so that the output presents a false level to the load. When the input goes true, VT1 conducts causing VT2 to be reverse biased and present a true level to the load. C1 charges through R3 and R4 and VT2 again becomes forward biased. The time for this to occur is adjusted on test to a value of 2.27 ms by selecting the value of R3.

5.3 Stabiliser.

The circuit uses +28V d.c. to produce a +10V d.c. supply with a stability of ± 5% and a regulation of better than 1% for a 30 mA load current.

Changes in the output voltage are sensed by the resistor chain R6, R7 and R8. The value of R6 is selected on test and is wired in parallel with R7 if the output is greater than 10. 5V, and in parallel with R8 if the output is less than 9. 5V. The sensed voltage controls the bias on VT1, the emitter of this transistor being held at a reference level of 6. 8V by zener diode MR1. Control of the current through VT1 varies the drive to VT2 and hence the level of the output voltage.

The two transistors are protected from a large reverse bias by diodes MR3 and MR4. The d. c. level on the base of VT2 is prevented from rising above 13V by the zener diode MR2.

Chapter 6: MAINTENANCE AND TEST PROGRAMS

6.1 Maintenance.

Details of maintenance and the tools and lubricants required, are as stated in the manufacturer's handbooks. A set of handbooks, tools and lubricants is supplied with each teleprinter.

NOTE: Lifting by diagonally opposite corners and excessive jolting or tilting may upset adjustments. Once installed and set up, the teleprinter should be disturbed as little as possible.

6.2 Test Program.

A diagnostic program is not provided for the teleprinter. On completion of maintenance checks, the operators daily test program X50 should be run to ensure the correct functioning of the equipment. X50 is described in Section 3.1.3.

NOTE: In any teleprinter test program a Carriage Return instruction must be followed by a Space or Line Feed instruction. If this procedure is not observed, the teleprinter may attempt to type a character during the carriage return time.